IN THE CLAIMS

1-19. (Canceled)

20. (New) An array substrate for in-plane switching mode liquid crystal display device, comprising:

a substrate having a plurality of pixel regions;

a plurality of gate lines, a gate electrode, a plurality of common lines and a common electrode on the substrate;

a first insulating layer over the substrate;

a semiconductor layer on the first insulating layer;

a plurality of data lines, source and drain electrodes and a pixel electrode on the semiconductor layer, the common line and the pixel electrode being formed a first storage capacitor;

a second insulating layer over the substrate; and

an auxiliary line on the second insulating layer and being overlapped with the common line, the pixel electrode and the auxiliary line being formed a second storage capacitor.

21. (New) The array substrate according to claim 20, further comprising a dummy line in a non-display area of the substrate.

22. (New) The array substrate according to claim 21, wherein the dummy line communicates with the auxiliary line.

23. (New) The array substrate according to claim 21, wherein the dummy line includes one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

24. (New) The array substrate according to claim 20, wherein the auxiliary line includes one of Indium-Tin-Oxide (ITO) and Indium Zinc Oxide (IZO).

25. (New) The array substrate according to claim 20, wherein the gate line, the common line and the common electrode are formed using the same material on a same layer.

26. (New) The array substrate according to claim 20, wherein the gate line, the common line and the common electrode includes one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

27. (New) The array substrate according to claim 20, further comprising an insulating layer between the common line and the pixel electrode to form a first auxiliary storage capacitor.

28. (New) The array substrate according to claim 27, wherein the insulating layer includes one of silicon nitride (SiNx) and silicon oxide (SiO_2).

29. (New) The array substrate according to claim 20, further comprising an insulating layer between the pixel electrode and the auxiliary line to form a second auxiliary storage capacitor.

30. (New) The array substrate according to claim 29, wherein the insulating layer includes one of silicon nitride (SiNx) and silicon oxide (SiO_2).

31. (New) The array substrate according to claim 20, wherein the thin film transistor having a gate electrode, an active layer, a source electrode and a drain electrode.

32. (New) A method for fabricating an array substrate for in-plane switching mode liquid crystal display device, comprising:

forming a plurality of gate lines, a gate electrode, a plurality of common lines, a common electrode and a dummy line on a substrate, the dummy line being formed in a non-display area;

forming a first insulating layer over the substrate;

forming a semiconductor layer on the first insulating layer;

forming a plurality of data lines, source and drain electrodes and a pixel electrode on the semiconductor layer;

forming a second insulating layer over the substrate; and

forming an auxiliary line on the second insulating layer, the auxiliary line being overlapped with the common line and one end of the auxiliary line communicating with the dummy line.

33. (New) The method according to claim 32, wherein the gate line, the common line and the dummy line are formed using the same material on a same layer.

34. (New) The method according to claim 32, wherein the gate line, the common line and the dummy line are formed of one of aluminum (Al), aluminum alloy (Al alloy), tungsten (W), molybdenum (Mo), copper (Cu) and chromium (Cr).

35. (New) The method according to claim 32, wherein the auxiliary line is formed of one of Indium-Tin-Oxide (ITO) and Indium Zinc Oxide (IZO).

36. (New) The method according to claim 32, wherein the first insulating layer is formed of one of silicon nitride (SiNx) and silicon oxide (SiO_2).

37. (New) The method according to claim 32, wherein the second insulating layer is formed of one of silicon nitride (SiNx) and silicon oxide (SiO_2).

38. (New) The method according to claim 32, wherein the common line and the pixel electrode to form a first storage capacitor.

39. (New) The method according to claim 32, wherein the pixel electrode and the auxiliary line to form a second storage capacitor.